

Advanced Chip Design Practical Examples In Verilog

A Practical Guide for SystemVerilog Assertions SystemVerilog for Design Second Edition Learning from VLSI Design Experience Verilog® Quickstart Java by Example Rapid Prototyping of Digital Systems Formal Methods in Computer-aided Design Hardware Verification with System Verilog Verilog and SystemVerilog Gotchas Specification-driven Functional Verification with Verilog PLI & VPI and SystemVerilog DPI IEEE Circuits & Devices Verilog Computer-Based Training Course Java Studio by Example Proceedings of the ... IEEE International Caracas Conference on Devices, Circuits and Systems Effective VisualAge for Java, Version 3 Proceedings Reuse Methodology Manual for System-on-a-chip Designs Core Java Instant Java Nuts & Volts Srikanth Vijayaraghavan Stuart Sutherland Weng Fook Lee James M. Lee Jerry R. Jackson James O. Hamblen Mike Mintz Stuart Sutherland Suraj N. Kurapati Zainalabedin Navabi Lynn Weaver Scott Stanchfield Michael Keating Gary Cornell John A. Pew

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systemverilog language consists of three very specific areas of constructs design assertions and testbench assertions add a whole new dimension to the asic verification process assertions provide a better way to do verification proactively traditionally engineers are used to writing verilog test benches that help simulate their design verilog is a procedural language and is very limited in capabilities to handle the complex asic s built today systemverilog assertions sva are a declarative and temporal language that provides excellent control over time and

parallelism this provides the designers a very strong tool to solve their verification problems while the language is built solid the thinking is very different from the user s perspective when compared to standard verilog language the concept is still very new and there is not enough expertise in the field to adopt this methodology and be successful while the language has been defined very well there is no practical guide that shows how to use the language to solve real verification problems this book will be the practical guide that will help people to understand this new methodology today s soc complexity coupled with time to market and first silicon success pressures make assertion based verification a requirement and this book points the way to effective use of assertions satish s iyengar director asic engineering crimson microsystems inc this book benefits both the beginner and the more advanced users of systemverilog assertions sva first by introducing the concept of assertion based verification abv in a simple to understand way then by discussing the myriad of ideas in a broader scope that sva can accommodate the many real life examples provided throughout the book are especially useful irwan sie director ic design ess technology inc systemverilogassertions is a new language that can find and isolate bugs early in the design cycle this book shows how to verify complex protocols and memories using sva with seeral examples this book is a good reference guide for both design and verification engineers derick lin senior director engineering airgo networks inc

systemverilog is a rich set of extensions to the ieee 1364 2001 verilog hardware description language verilog hdl these extensions address two major aspects of hdl based design first modeling very large designs with concise accurate and intuitive code second writing high level test programs to efficiently and effectively verify these large designs the first edition of this book addressed the first aspect of the systemverilog extensions to verilog important modeling features were presented such as two state data types enumerated types user degined types structures unions and interfaces emphasis was placed on the proper usage of these enhancements for simulation and synthesis systemverilog for design second edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard it is important that the book reflect these syntax and semantic changes to the systemverilog language in addition the second edition features a new chapter that explanis the systemverilog packages a new appendix that summarizes the synthesis guidelines presented throughout the book and all of the code examples have been updated to the final syntax and rerun using the latest version of the synopsys mentor and cadance tools

this book shares with readers practical design knowledge gained from the author s 24 years of ic design experience

the author addresses issues and challenges faced commonly by ic designers along with solutions and workarounds guidelines are described for tackling issues such as clock domain crossing using lockup latch to cross clock domains during scan shift implementation of scan chains across power domain optimization methods to improve timing how standard cell libraries can aid in synthesis optimization bkm best known method for rtl coding test compression memory bist usage of signed verilog for design requiring ve and ve calculations state machine code coverage and much more numerous figures and examples are provided to aid the reader in understanding the issues and their workarounds

verilog quickstart has been revised and updated in accordance with the new ieee 1364 1999 standard much of which applies to synthesizable verilog new examples have been included as well as additional material added throughout

this book highlights key features of the java language with examples designed for experienced programmers the text clearly and concisely describes how to create java applets and applications and shows the development of a complete java program from start to finish the cd rom includes all java source code examples from the book java applets the latest release of the java developer s kit and cafe lite

new to this edition is an introduction to embedded operating systems for soc designs featuring four accelerated tutorials on the quartus ii and nios ii design environments this edition progresses from introductory programmable logic to full scale soc design integrating hardware implementation software development operating system support state of the art i o and ip cores this edition features altera s new 7 1 quartus ii cad and nios ii soc tools and includes projects for altera s de1 de2 up3 up2 and up1 fpga development boards

this is the second of our books designed to help the professional verifier manage complexity this time we have responded to a growing interest not only in object oriented programming but also in systemverilog the writing of this second handbook has been just another step in an ongoing masochistic endeavor to make your professional lives as painfree as possible the authors are not special people we have worked in several companies large and small made mistakes and generally muddled through our work there are many people in the industry who are smarter than we are and many coworkers who are more experienced however we have a strong desire to help we have been in the lab when we bring up the chips fresh from the fab with customers and sales breathing down our

necks we've been through software 1 bring up and worked on drivers that had to work around bugs in production chips what we feel makes us unique is our combined broad experience from both the software and hardware worlds mike has over 20 years of experience from the software world that he applies in this book to hardware verification robert has over 12 years of experience with hardware verification with a focus on environments and methodology

in programming gotcha is a well known term a gotcha is a language feature which if misused causes unexpected and in hardware design potentially disastrous behavior the purpose of this book is to enable engineers to write better verilog systemverilog design and verification code and to deliver digital designs to market more quickly this book shows over 100 common coding mistakes that can be made with the verilog and systemverilog languages each example explains in detail the symptoms of the error the languages rules that cover the error and the correct coding style to avoid the error the book helps digital design and verification engineers to recognize these common coding mistakes and know how to avoid them many of these errors are very subtle and can potentially cost hours or days of lost engineering time trying to find and debug the errors this book is unique because while there are many books that teach the language and a few that try to teach coding style no other book addresses how to recognize and avoid coding errors with these languages

an insider's guide to writing java powered pages with javastudio this book shows how without writing a single line of code the hands on format can be used as both a tutorial and reference depending on the experience level the cd rom contains a full working 30 day try and buy version of javastudio

a practical guide to the latest features of versions 3.02 and 3.5 and a valuable resource for ibm's visualage for java certification program ibm's visualage for java is one of the leading tools available for building java and javabeans applications currently ibm's visualage for java certification programs are offered all over the world written by ibm insiders this book focuses on the more advanced topics related to visualage for java and prepares readers for the certification program readers learn visualage for java's ide and how to use the language for enterprise data access and transaction processing cd rom contains ibm visualage for java entry edition sun java 2 and all the code examples from the book

the asian test symposium provides an international forum for engineers and researchers from all countries of the world especially from asia to present and discuss various aspects of system board and device testing with design

manufacturing and field considerations in mind at's 2003's papers shares state of the art ideas and technologies in testing

silicon technology now allows us to build chips consisting of tens of millions of transistors this technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer as a result many ASIC developers and silicon vendors are re-examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available design reuse the use of pre-designed and pre-verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity reuse methodology manual for system on a chip designs second edition outlines an effective methodology for creating reusable designs for use in a system on a chip soc design methodology silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process

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